REMARKS

This response is intended as a full and complete response to the non-final Office Action mailed July 12, 2005. In the Office Action, the Examiner notes that claims 1-20 are pending and rejected. By this response, the Applicant has herein amended claims 1-4, 7-8, 10-14, 17, and 18-20. Claims 5, 9, and 15-16 continue unamended. Claim 6 is hereby cancelled. No new matter has been entered.

In view of the foregoing amendments and the following discussion, Applicant submits that none of the claims now pending in the application are indefinite or obvious under the provisions of 35 U.S.C. §§112 or 103. Thus, Applicant believes that all these claims are now in allowable form.

It is to be understood that Applicant, by amending the claims, does not acquiesce to the Examiner's characterizations of the art of record or to Applicant's subject matter recited in the pending claims. Further, Applicant is not acquiescing to the Examiner's statements as to the applicability of the prior art of record to the pending claims by filing the instant responsive amendments.

INFORMATION DISCLOSURE STATEMENT

A proper Information Disclosure Statement pursuant to 37 C.F.R. 1.98(b) is submitted herewith. The Applicant was unable to determine the exact publication date of the Hewlett Packard 3787B Technical Manual containing the DS1 Interface Card diagram, however, Applicant is reasonably certain that the publication date of the Hewlett Packard 3787B Technical Manual is on or prior to January 1, 1990.

CLAIM OBJECTIONS

The Examiner has objected to claims 2-14 and 20 for various informalities.

With respect to claims 2-4 and 6, Applicant has herein amended claims 2-4 to clearly identify the circuitry being referenced, and Applicant has herein amended claim 6.

With respect to claim 7, Applicant has herein amended claim 7 to indicate that the at least two resistors in series form a resistor chain where one end of the resistor chain is coupled to one of the input terminals and the other end of the resistor is coupled to another of the input terminals, as depicted and described in FIG. 1 of Applicant's specification as filed.

With respect to claims 8, 10-13, and 20, Applicant has herein amended claims 8, 10-13, and 20 to clearly identify the circuitry being referenced.

Therefore, Applicant respectfully requests that the Examiner's objections be withdrawn.

REJECTIONS

35 U.S.C. §112

The Examiner has rejected claims 7, 12, 14 and 17 under 35 U.S.C. §112, ¶2, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response, with respect to claims 7 and 12, Applicant has herein amended claims 7 and 12 to clarify the configuration of the resistors in series.

In response, with respect to claim 14, Applicant has herein amended claim 14 to clarify the configuration of the capacitors in series.

In response, with respect to claim 17, Applicant has herein amended claim 17 to indicate that at least a portion of at least one of the impedance load circuitry, the amplifying circuitry, and the impedance matching circuitry may be configured to adjust the gain of the circuit. As taught in Applicant's specification as originally filed, "[t]he gain of the tap circuit 100 can be adjusted by varying resistors R3, R4, resistors R5, R6, R7, or resistors R8, R9." (Specification, Page 7, Lines 6-7). As such, various combinations of the impedance load circuitry, the amplifying circuitry, and the impedance matching circuitry may be configured for adjusting the gain of the tap circuit.

Accordingly, Applicant submits that claims 7, 12, 14 and 17 fully satisfy the requirements of 35 U.S.C. §112 and are patentable thereunder. Therefore, Applicant respectfully requests that the Examiner's rejection be withdrawn.

35 U.S.C. § 103

Claims 1-14 and 17-20

The Examiner has rejected claims 1-14 and 17-20 under 35 U.S.C. §103(a) as being unpatentable over McEwan (U.S. 5,519,342, hereinafter "McEwan"). The rejection is respectfully traversed.

In general, McEwan teaches a transient digitizer with displacement current samplers. As taught in McEwan, the transient digitizer uses a signal transmission line, a strobe transmission line, and a plurality of sample gates connected to the signal transmission line. (McEwan, Col. 3, Ln. 5-7). McEwan, however, does not teach Applicant's invention of at least claim 1, as a whole. Namely, McEwan fails to teach or suggest at least the limitations of "wherein the impedance load circuitry comprises circuitry configured to provide a dissipation load for the received transmission signal" and "wherein the circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry," as taught in Applicant's invention of at least claim 1. In particular, Applicant's claim 1 positively recites:

> A transmission line tap circuit, comprising:
> at least two input terminals configured for coupling to a transmission line;
> impedance load circuitry configured to provide an impedance load to the transmission line for tapping the transmission line and receiving a transmission signal propagating there through, wherein the impedance load circuitry comprises circuitry configured to provide a dissipation load for the received transmission signal;
> amplifying circuitry configured to amplify the received transmission signal and directly connected to the impedance load circuitry, wherein the circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry;

> impedance matching circuitry configured to provide an impedance match to an impedance load of at least one Line Interface Unit (LIU) and directly connected to a plurality of outputs of the amplifying circuitry; and
>
> at least two output terminals configured for coupling said transmission signal to the at least one LIU and directly connected to the impedance matching circuitry.
> (Emphasis added.)

As such, Applicant's invention of at least claim 1 teaches a transmission line tap circuit. The transmission line tap circuit includes impedance load circuitry configured to provide an impedance load to the transmission line for tapping the transmission line and receiving a transmission signal propagating there through. As taught in Applicant's invention of at least claim 1, the impedance load circuitry includes circuitry configured to provide a dissipation load for the received transmission signal. The circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry.

In the Office Action, the Examiner asserts that sampler gate 213 may be replaced with sampler 351 for teaching the impedance load circuitry of Applicant's invention of claim 1. The Examiner further asserts that the amplifiers 217 may be replaced with FET buffer 368 and amplifier 375 for teaching the amplifying circuitry of Applicant's invention of claim 1. The Applicant respectfully disagrees.

As taught in FIG. 6 of McEwan, the transmission line 212 is coupled to input terminals associated with each sampler gate 213. The sampler gates 213 are coupled to respective input terminals of amplifier circuits 217. The sampler gates 213 include Schottky diodes. A sampler gate of diodes, as taught in McEwan, is not impedance load circuitry configured to provide an impedance load, as taught in Applicant's invention of at least claim 1. Similarly, a sampler gate of diodes, as taught in McEwan, is not circuitry configured to provide a dissipation load, as taught in Applicant's invention of at least claim 1. Furthermore, with respect to FIG. 6 of McEwan, the output of each of the sampler gates 213 is coupled to the respective input terminals of the amplifier circuits 217. As taught in McEwan, however, the only component associated with the connection between sampler 213 and amplifier

circuit 217 is a capacitor 216. The capacitor 216 simply cannot provide a dissipation load. As such, McEwan fails to teach or suggest circuitry configured to provide a dissipation load for the received transmission signal, as taught in Applicant's invention of at least claim 1.

Furthermore, McEwan teaches that samplers 213 tap the input transmission line in parallel. In other words, McEwan teaches that each pair samplers 213 and amplifying circuits 217 operates independently from every other pair of samplers 213 and amplifying circuits 217. In fact, McEwan fails to teach or suggest any circuitry configured for controlling combinations of the pairs of samplers 213 and amplifying circuits 217. By contrast, Applicant's invention teaches that the circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry. In other words, in Applicant's invention of at least claim 1, varying voltages are provided to at least two input terminals of the amplifying circuitry by dissipation load circuitry associated with at least two input terminals. As such, McEwan fails to teach or suggest circuitry configured to provide a dissipation load, and that the circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry, as taught in Applicant's invention of at least claim 1.

As taught in FIG. 8 of McEwan, the transmission line 350 is coupled to an input terminal 352. The input terminal 352 is in turn coupled to sampler 351. As taught in McEwan, sampler 351 includes four diodes configured in a bridge having four terminals. A first terminal of the bridge is connected across a positive strobe resistor 358 to a positive strobe transmission line 359. A third terminal is coupled across a negative strobe resistor 361 to a negative strobe transmission line 362. (McEwan, Col. 10, Lines 20-29). A sampler gate of diodes coupled to an input transmission line and a pair of strobe transmission lines for sampling the input transmission line simply cannot operate as circuitry configured to provide a dissipation load, as taught in Applicant's invention of at least claim 1.

Furthermore, as taught in McEwan, the sampler 351 is also coupled to a FET buffer 368. In particular, McEwan teaches that the terminal of sampler 351 that is connected to the FET buffer is coupled to capacitor 365. The terminal of sampler 351 that is connected to the FET buffer 368 is coupled to FET buffer 368 through resistor 367. In particular, McEwan states that "[t]he output of the sampler is supplied across line 366 through resistor 367 to the gate of FET buffer 368. Also, resistor 369 is connected from the gate of FET buffer 368 to ground." (McEwan, Col. 10, Lines 60-62). In other words, McEwan merely teaches that the charge holding capacitance 365 supplies the sample signal to FET buffer 368 via line 366. McEwan is completely devoid of any teaching or suggestion of circuitry configured to provide a dissipation load for a received transmission signal.

Furthermore, even assuming McEwan did teach circuitry configured to provide a dissipation load for a received transmission signal (which Applicant maintains it does not), McEwan would still fail to teach Applicant's limitation that the circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry. In fact, even the replacement of the samplers 213 and amplifiers 217 of McEwan with samplers 351, FETs 368, and amplifiers 375 of McEwan, as suggested by the Examiner, would still fail to teach or suggest Applicant's invention of claim 1, as a whole. As described herein, each sampler 213 samples transmission line 212, in parallel, at different points along the transmission line. As such, replacement of samplers 213 and amplifiers 217 would still teach that each pair of samplers 351, FETs 368, and amplifiers 375 operates independently from every other pair of samplers 351, FETs 368, and amplifiers 375. In other words, in such a configuration the samplers would still tap the input transmission line in parallel, as well as independently from each other. Thus, independent circuitry associated with each of the samplers, configured for obtaining parallel taps of the input transmission line, as taught in McEwan, cannot teach circuitry configured to provide a dissipation load for providing at least two varying voltages to at least two input terminals of amplifying circuitry, as taught in Applicant's invention of at least claim 1.

As such, McEwan is completely devoid of any teaching or suggestion of circuitry configured to provide a dissipation load for the received transmission signal where the impedance load circuitry comprises circuitry configured to provide a dissipation load for the received transmission signal, as taught in Applicant's invention of at least claim 1. Thus, McEwan fails to teach or suggest Applicant's invention, as a whole.

The test under 35 U.S.C. §103 is not whether an improvement or a use set forth in a patent would have been obvious or non-obvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 110 USPQ 1021, 1024 (Fed. Cir. 1984) (emphasis added). Moreover, the invention as a whole is not restricted to the specific subject matter claimed, but also embraces its properties and the problem it solves. In re Wright, 6 USPQ 2d 1959, 1961 (Fed. Cir. 1988) (emphasis added). The McEwan reference fails to teach or suggest Applicant's invention as a whole.

As such, the Applicant submits that independent claim 1 is not obvious and fully satisfies the requirements of 35 U.S.C. §103 and is patentable thereunder. Furthermore, independent claims 18 and 20 recite features substantially similar to the features of independent claim 1. As such, for at least the reasons discussed with respect to claim 1, Applicant submits that independent claims 18 and 20 are also not obvious and fully satisfy the requirements of 35 U.S.C. §103 and are patentable thereunder.

As such, Applicant submits that independent claims 1, 18 and 20 are not obvious and fully satisfy the requirements of 35 U.S.C. §103 and are patentable thereunder. Furthermore, claims 2-14, 17 and 19 depend directly or indirectly from independent claims 1, 18, and 20, and recite additional features therefor. Thus, for at least the same reasons as discussed above, Applicant submits that these dependent claims are also not obvious and fully satisfy the requirements of 35 U.S.C. §103 and are patentable thereunder. Therefore, Applicant respectfully requests that the Examiner's rejection be withdrawn.

Claims 15 and 16

The Examiner has rejected claims 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over McEwan in view of Song (US 4,087,754, hereinafter "Song"). The rejection is respectfully traversed.

For at least the reasons discussed above with respect to independent claim 1, from which claims 15 and 16 depend, Applicant's invention is non-obvious and patentable over McEwan under 35 U.S.C. §103(a). Furthermore, Song fails to bridge the substantial gap between McEwan and Applicant's invention.

In general, Song discloses a digital to analog converter. In particular, Song discloses conversion of analog signals into linear delta modulated signals, and the compression of the linear delta modulated signals into compressed pulse code modulated signals. Song, however, fails to teach or suggest Applicant's invention of at least claim 1, as a whole. Song is completely devoid of any teaching or suggestion of at least the limitations of "wherein the impedance load circuitry comprises circuitry configured to provide a dissipation load for the received transmission signal" and "wherein the circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry," as taught in Applicant's invention of at least claim 1. Rather, the Examiner merely relies upon Song for teaching T1 and E1 transmission lines.

As such, Applicant submits that independent 1 is not obvious and fully satisfies the requirements of 35 U.S.C. §103 and is patentable thereunder. Furthermore, claims 15 and 16 depend directly from independent claim 1 and recite additional features therefor. Accordingly, for at least the same reasons as discussed above, Applicant submits that dependent claims 15 and 16 are not obvious and fully satisfy the requirements of 35 U.S.C. §103 and are patentable thereunder. Therefore, Applicant respectfully requests that the Examiner's rejection be withdrawn.

CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are indefinite or obvious under the provisions of 35 U.S.C. §§112 or 103. Consequently, Applicant believes that all of these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Mr. Eamon J. Wall, Esq at (732) 383-1438 or Mr. Michael Bentley at (732) 383-1434 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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